CLAIMS

What is claimed is:

1. A display driver comprising:
   a display;
   a first display driver integrated circuit having a first plurality of channels coupled to said display; and
   a second display driver integrated circuit having a second plurality of channels coupled to said display wherein control signals from said first display driver integrated circuit for enabling said display to receive video information from said first plurality of channels are phase adjusted to control signals from said second display driver integrated circuit for enabling said display to receive video information from said second plurality of channels to prevent visual artifacts on said display.

2. The system as recited in claim 1 further including:
   a first memory coupled to said first display driver integrated circuit for storing video information; and
   a second memory coupled to said second display driver integrated circuit for storing video information.

3. The system as recited in claim 2 wherein said display is a liquid crystal microdisplay.

4. The system as recited in claim 3 further including a phase lock loop to compare a clock signal of said first display driver integrated circuit to a clock signal of said second display driver integrated circuit wherein said clock signal of said first display driver integrated circuit has an equal frequency as said clock signal of said second display driver integrated circuit and wherein said phase lock loop generates an error signal used to reduce a phase difference between said clock signals of said first and second driver integrated circuits.

5. The system as recited in claim 4 wherein said first display driver integrated circuit comprises:

a digital processing section for receiving and processing digital video information;

an analog conversion section coupled to said digital processing section wherein said analog conversion section converts digital video information to analog video information that is provided to said first plurality of channels; and

a timing/clock section coupled to said digital processing section, said analog conversion section, said first memory, and said display.

6. The system as recited in claim 5 wherein said second display driver integrated circuit comprises:

a digital processing section for receiving and processing digital video information;

an analog conversion section coupled to said digital processing section wherein said analog conversion section converts digital video information to analog video information that is provided to said second plurality of channels; and

a timing/clock section coupled to said digital processing section, said analog conversion section, said first memory, and said display.

7. The system as recited in claim 6 wherein said first and second display driver integrated circuits each generate a frame synchronization signal to indicate when said first and second display driver integrated circuits are prepared to process video information.

8. The system as recited in claim 7 wherein said first and second display driver integrated circuits each generate a frame polarity signal to indicate a polarity of analog video information being provided to said display.

9. The system as recited in claim 8 wherein calibration of digital to analog converters of said second display driver integrated circuit is performed using reference voltages and comparators from said first display driver integrated circuit.

10. A method for driving a liquid crystal microdisplay comprising the steps of:

coupling at least one channel from a first display driver integrated circuit to the liquid crystal microdisplay;

coupling at least one channel from a second display driver integrated circuit to the liquid crystal microdisplay;

comparing a frame synchronization signal from said first and second display driver integrated circuits; and

initiating a transfer of video information through said at least one channel of said first and second display driver integrated circuits to the liquid crystal microdisplay when said frame synchronization signals indicate said first and second display driver integrated circuits are both prepared to transfer video information together to the liquid crystal microdisplay.

11. The method for driving a liquid crystal microdisplay as recited in claim 10 further including the steps of:

comparing a frame polarity signal from said first and second display driver integrated circuits;

preventing said transfer of video information to the liquid crystal microdisplay if a polarity of said video information provided by said first display driver integrated circuit differs from a polarity of said video information provided by said second display driver integrated circuit; and

correcting said polarity difference of said video information between said first and second display driver integrated circuits.

12. The method for driving the liquid crystal microdisplay as recited in claim 11 further including the steps of:

comparing a phase shift between internal clock signals of said first and second display driver integrated circuits; and

adjusting said internal clock signals of said first and second display driver integrated circuits to reduce said phase shift to prevent visual artifacts on the liquid crystal microdisplay.

13. The method for driving the liquid crystal microdisplay as recited in claim 12 further including the steps of:

providing timing signals to the liquid crystal microdisplay for transferring video information through said at least one channel of said first display driver integrated circuit wherein said timing signals is said internal clock or derived from said internal clock signal of said first display driver integrated circuit; and

providing timing signals to the liquid crystal microdisplay for transferring video information through said at least one channel of said second display driver integrated circuit wherein said timing signals is said internal clock signal of said second display driver integrated circuit.

14. The method for driving the liquid crystal microdisplay as recited in claim 13 further including the steps of:

calibrating digital to analog converters of said first display driver integrated circuit periodically; and

calibrating digital to analog converters of said second display driver integrated circuit periodically using comparators and reference voltages from said first display driver integrated circuit.

15. A color display system comprising:

a first liquid crystal microdisplay;

a second liquid crystal microdisplay;

a third liquid crystal microdisplay;

a first display driver integrated circuit having a plurality of channel outputs for providing video information wherein said plurality of channel outputs is coupled to at least one of said first, second, or third liquid crystal microdisplay; and

a second display driver integrated circuit having a plurality of channel outputs for providing video information wherein said plurality of channel outputs is coupled to at least one of said first, second, or third liquid crystal microdisplays and wherein one of said first, second, or third microdisplays receives video information through channel outputs from both said first and second display driver integrated circuits.

16. The color display system as recited in claim 15 wherein an internal clock of said first display driver integrated circuit is compared to an internal clock of said second display driver integrated circuit and phase adjusted to reduce a delay between said internal clocks of said first and second display driver integrated circuits such that video information is stored substantially at the same time in said first, second, or third microdisplay that receives video information from both said first and second display driver integrated circuits to prevent visual artifacts.

17. The color display system as recited in claim 16 wherein video information is provided to said first and second display driver integrated circuits as digital video information.

18. The color display system as recited in claim 17 further including:

a first memory coupled to said first display driver integrated circuit for storing digital video information; and

a second memory coupled to said second display driver integrated circuit for storing digital video information.

19. The color display system as recited in claim 18 wherein digital to analog converters in said first and second display driver integrated circuits convert digital video information to analog video information for said first, second, and third liquid crystal microdisplays and wherein said digital to analog converters in said first and second display driver integrated circuits are calibrated periodically using same comparators and voltage references.

20. The color display system as recited in claim 19 wherein said first and second display driver integrated circuits do not transfer video information to said until both are synchronized to do so and wherein said first and second display driver integrated circuits do not transfer information when a polarity of video information differs.